Maintaining Status during Startup

The status of SR 25212 and thus the status of IR and LR area bits can be maintained when power is turned off and on by inserting the System Operation instruction (SYS(49)) into the program with the proper operand. If SYS(49) is used in this way, the status of SR 25212 will be preserved when power is turned off and on. If this is done and SR 25212 is ON, then the status of IR and LR area bits will also be preserved, as shown in the following table.

Status before shutdown		Status at next startup	
SR 25212	**SYS(49)**	**SR 25212**	**IR and LR bits**
ON	Executed	ON	Status maintained
	Not executed	OFF	Reset
OFF	Executed	OFF	Reset
	Not executed	OFF	Reset

Refer to *Section 5 Instruction Set* for details on SYS(49).

3-4-5 FAL (Failure Alarm) Area

A 2-digit BCD FAL code is output to bits 25300 to 25307 when the FAL or FALS instruction is executed. These codes are user defined for use in error diagnosis, although the PC also outputs FAL codes to these bits, such as one caused by battery voltage drop.

This area can be reset by executing the FAL instruction with an operand of 00 or by performing a Failure Read Operation from the Programming Console.

3-4-6 Battery Alarm Flag

SR bit 25308 is turned ON if the voltage of the CPU battery drops. The ALM indicator on the front of the CPU will also flash.

This bit can be programmed to activate an external warning for a low battery voltage.

The System Operation instruction (SYS(49)) can be used to turn off the operation of the battery alarm if desired, e.g., when DM 1000 to DM 1999 is placed in ROM and a battery is not used in operation. Refer to *Section 5 Instruction Set* for details.

3-4-7 Cycle Time Error Flag

SR bit 25309 is turned ON if the cycle time exceeds 100 ms. The ALM indicator on the front of the CPU will also flash. Program execution will not stop, however, unless the maximum time limit set for the watchdog timer is exceeded. Timers may become inaccurate after the cycle time exceeds 100 ms.

If the Cycle Time Set Enable Bit in the system parameter area is ON, the time used to determine a cycle time error, also in the system parameter area, can be set. Refer to *3-6 DM (Data Memory) Area* for details.

3-4-8 First Cycle Flag

SR bit 25315 is turned ON when PC operation begins and then turns OFF after one cycle of the program. The First Cycle Flag is useful in initializing counter values and other operations. An example of this is provided in *5-10 Timer and Counter Instructions*.

3-4-9 Clock Pulse Bits

Five clock pulses are available to control program timing. Each clock pulse bit is ON for the first half of the rated pulse time, then OFF for the second half, i.e., each clock pulse has a duty factor of 50%.